A2 cncld.

17. (New) The filter of claim 13 wherein the combinational circuit and the sequential circuit are interconnected to implement an infinite input response (IIR) filter.

REMARKS

Claims 5 and 6 have been amended to remove multiple claim dependencies, which are prohibited under U.S. patent law. New claims 8-17 are added.

All claims are believed in condition for allowance. Examination and allowance are kindly requested. The Examiner is kindly requested to address all future correspondence to Michael J. Donohue, Seed Intellectual Property Law Group PLLC, 701 Fifth Avenue, Suite 6300, Seattle, Washington 98104-7092.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made**."

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 5 and 6 have been amended as follows:

5. (Amended) The device as claimed in ~~any one of the preceding claims~~ claim 1 wherein coefficient lines CLin_0... Clin_n are not derived from a common input line but are instead respectively delayed by 0...n unit delays prior to input into said architecture [A].

6. (Amended) The device as claimed in ~~any preceding~~ claim 1 wherein instead of FA and FS elements, sequential adder and sequential subtractor elements are used.

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